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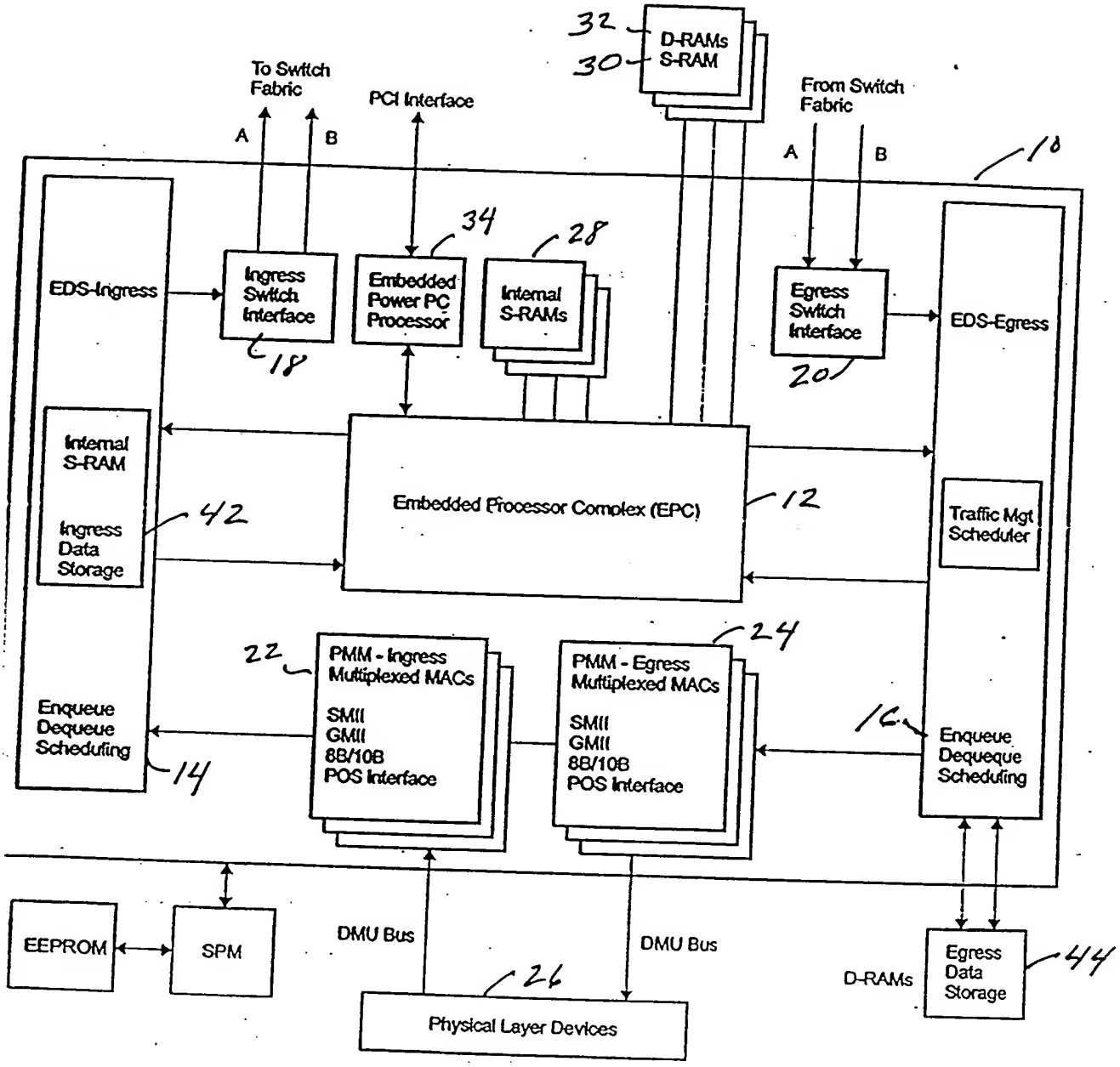
32
D-RAMs
30
S-RAM
To Switch Fabric
A
B
PCI Interface
From Switch Fabric
A
B
10
EDS-Ingress
Ingress Switch Interface
18
Embedded Power PC Processor
34
Internal S-RAMs
28
Egress Switch Interface
20
EDS-Egress
Internal S-RAM
Ingress Data Storage
42
Embedded Processor Complex (EPC)
12
Traffic Mgt Scheduler
22
PMM - Ingress Multiplexed MACs
SMII
GMII
8B/10B
POS Interface
24
PMM - Egress Multiplexed MACs
SMII
GMII
8B/10B
POS Interface
16
Enqueue Dequeue Scheduling
Enqueue Dequeue Scheduling
14
EEPROM
SPM
DMU Bus
DMU Bus
26
Physical Layer Devices
D-RAMs
Egress Data Storage
44

FIG. 1

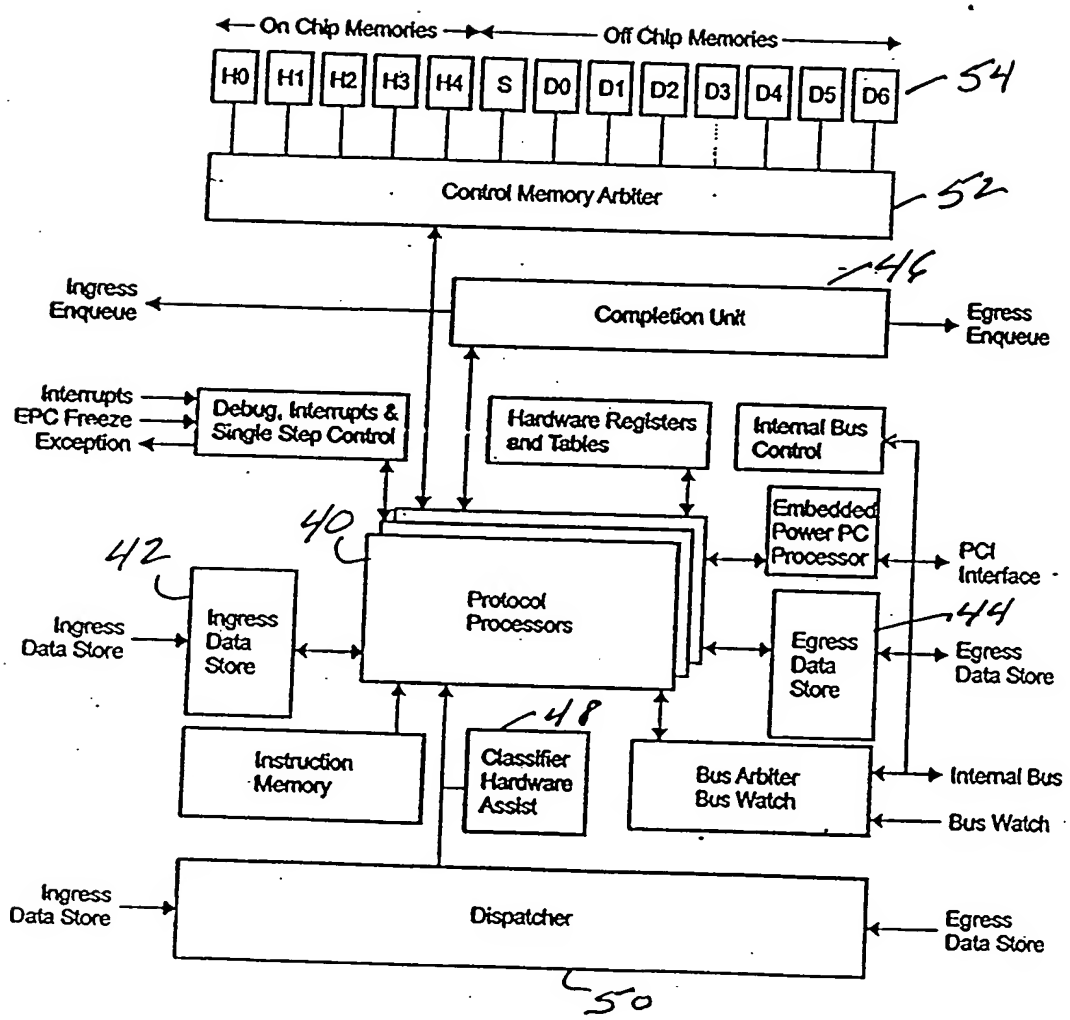
On Chip Memories
Off Chip Memories
H0
H1
H2
H3
H4
S
D0
D1
D2
D3
D4
D5
D6
54
Control Memory Arbiter
52
46
Ingress Enqueue
Completion Unit
Egress Enqueue
Interrupts
EPC Freeze
Exception
Debug, Interrupts & Single Step Control
Hardware Registers and Tables
Internal Bus Control
Embedded Power PC Processor
PCI Interface
40
42
Ingress Data Store
Ingress Data Store
Protocol Processors
Egress Data Store
44
Egress Data Store
48
Instruction Memory
Classifier Hardware Assist
Bus Arbiter Bus Watch
Internal Bus
Bus Watch
Ingress Data Store
Dispatcher
Egress Data Store
50

FIG. 2

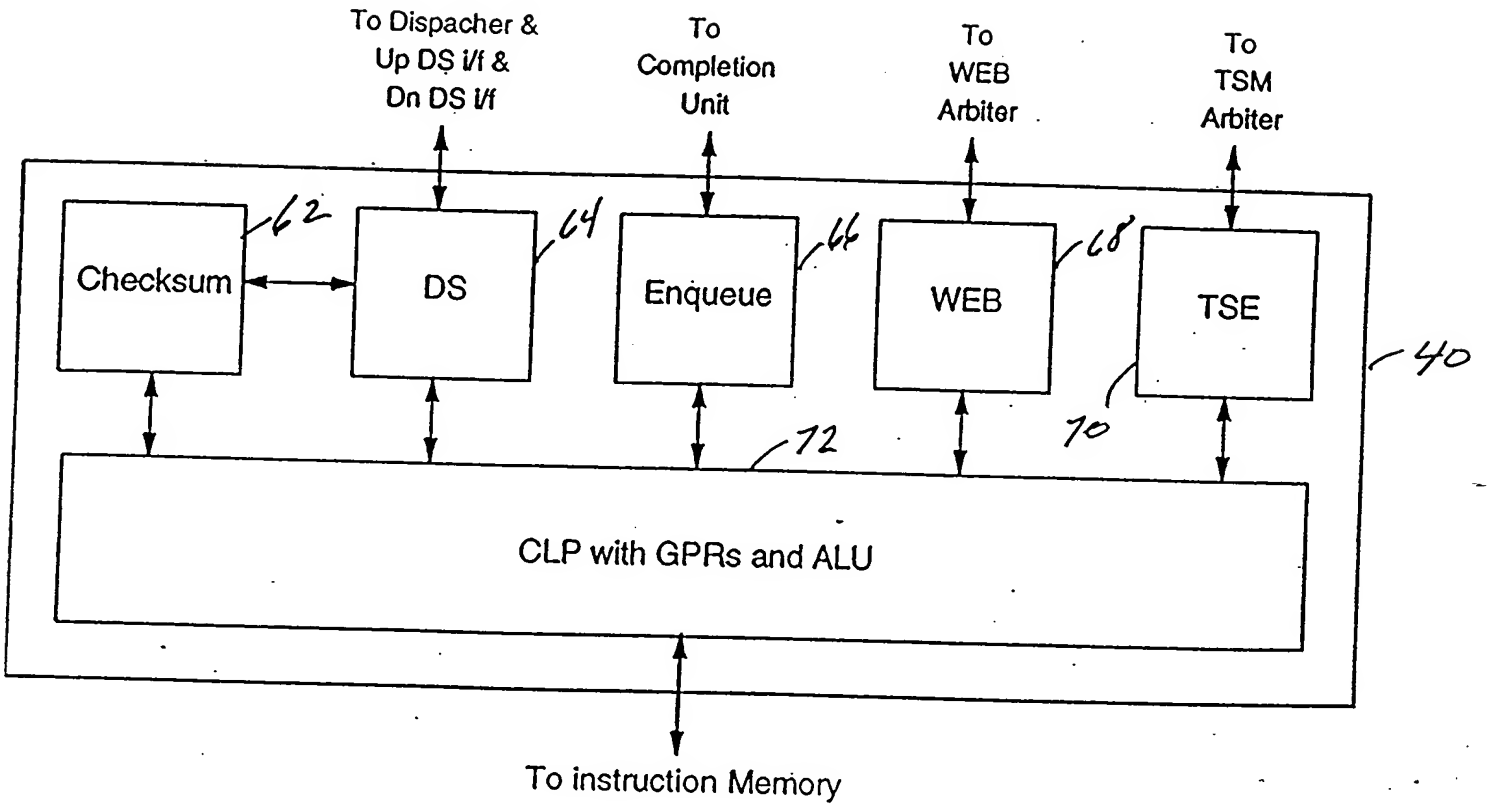
To Dispacher &
Up DS i/f &
Dn DS i/f
To
Completion
Unit
To
WEB
Arbiter
To
TSM
Arbiter
Checksum
62
DS
64
Enqueue
66
WEB
68
TSE
70
40
72
CLP with GPRs and ALU
To instruction Memory

FIG. 3

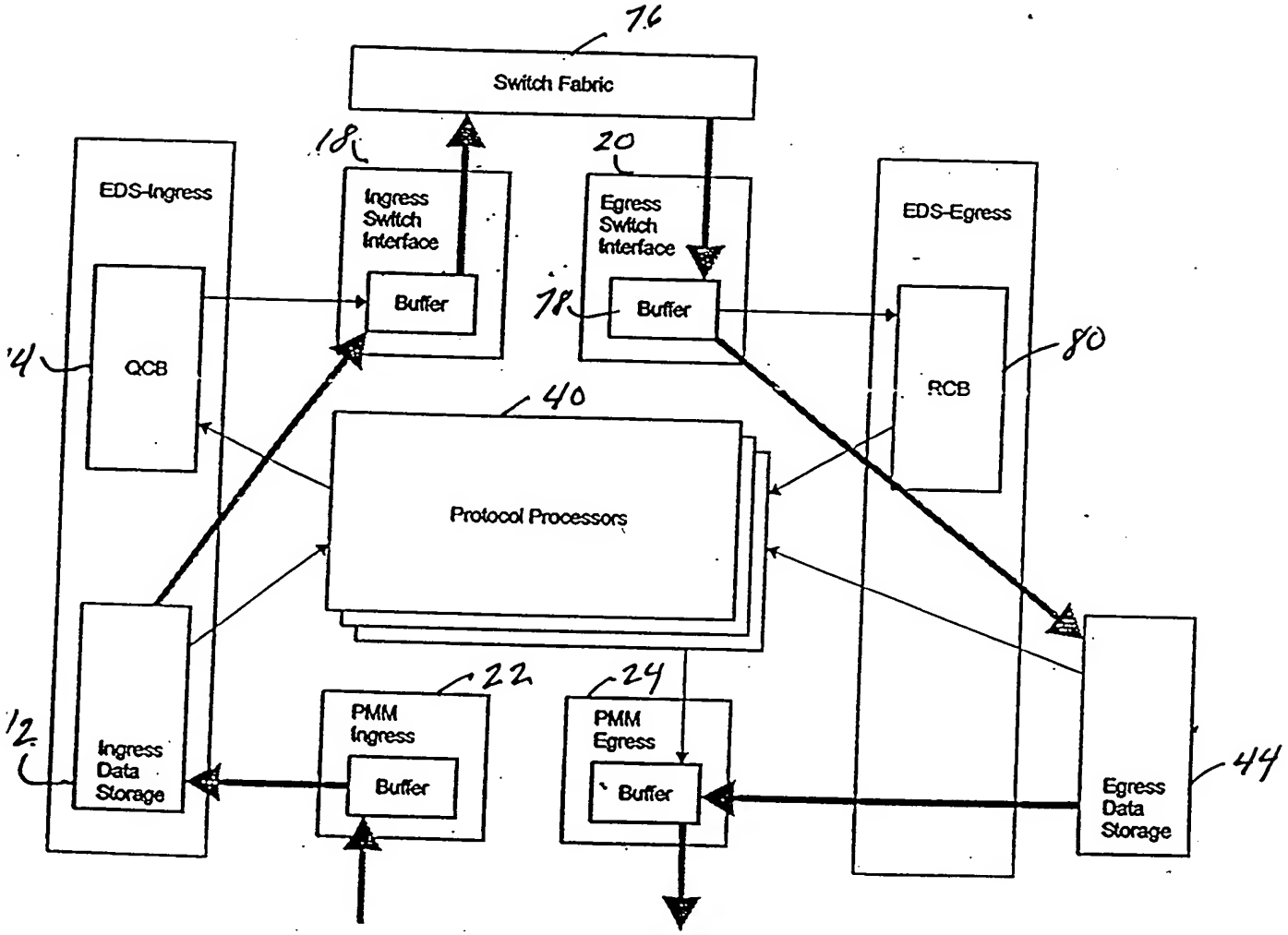
16
Switch Fabric
18
20
EDS-Ingress
Ingress Switch Interface
Egress Switch Interface
EDS-Egress
Buffer
Buffer
14
QCB
78
RCB
80
40
Protocol Processors
22
24
12
PMM Ingress
PMM Egress
Ingress Data Storage
Buffer
Buffer
Egress Data Storage
44

FIG. 4

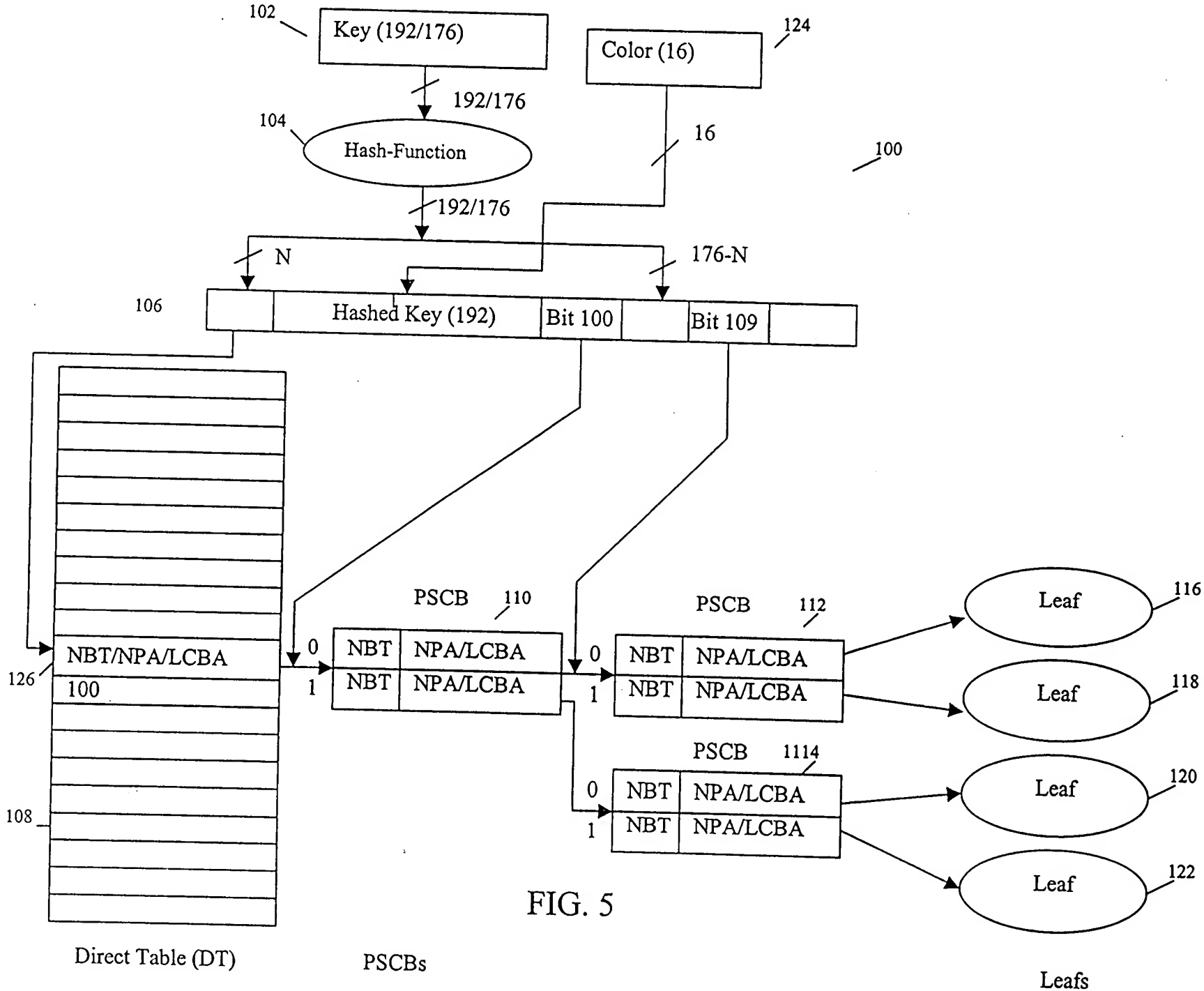

FIG. 5

RAL9-1999-0139-US1
Bass et al
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RAL9-1999-0129-US1
Bass, et al
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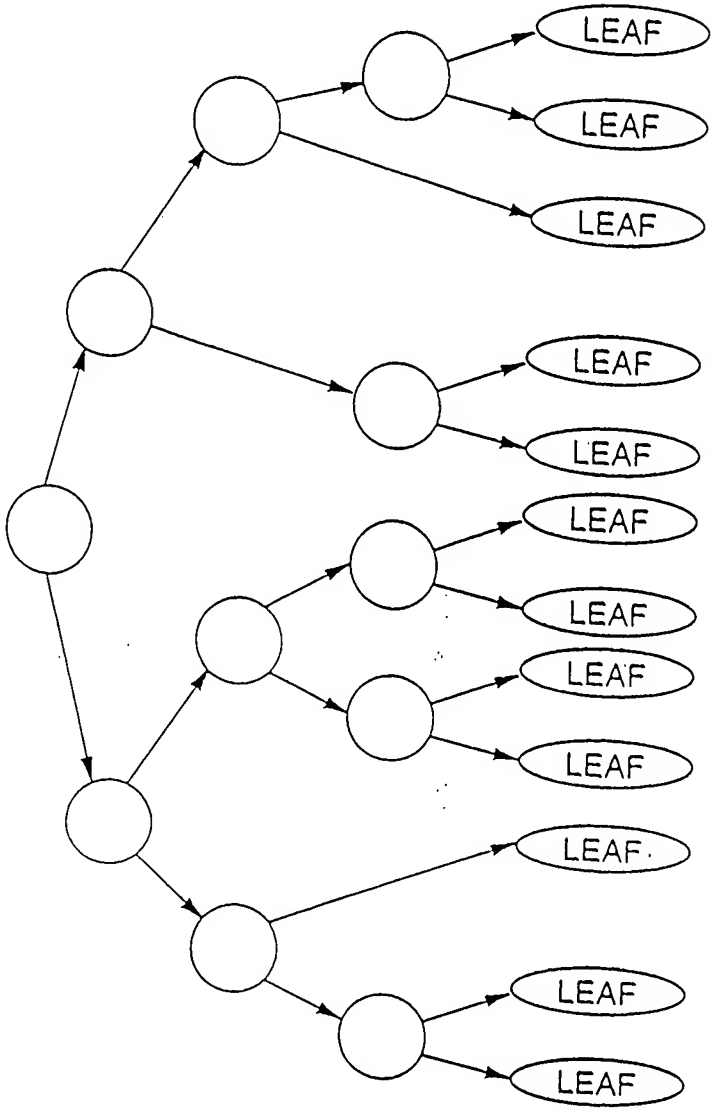
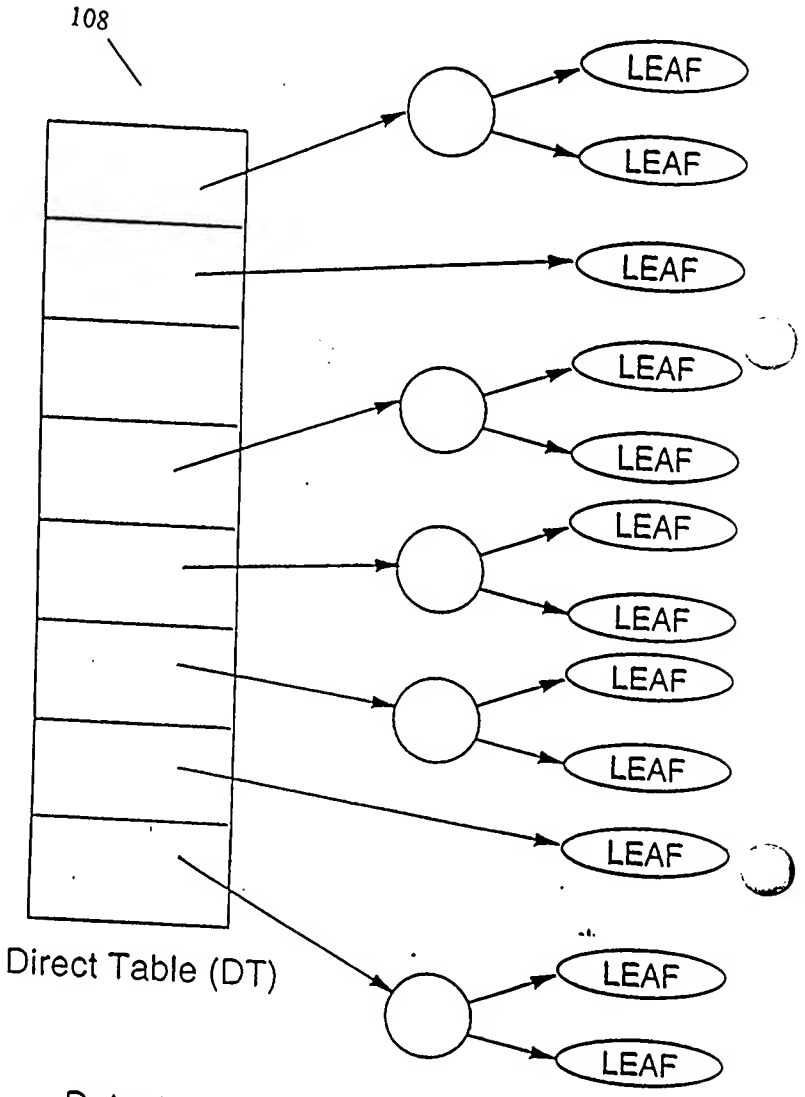
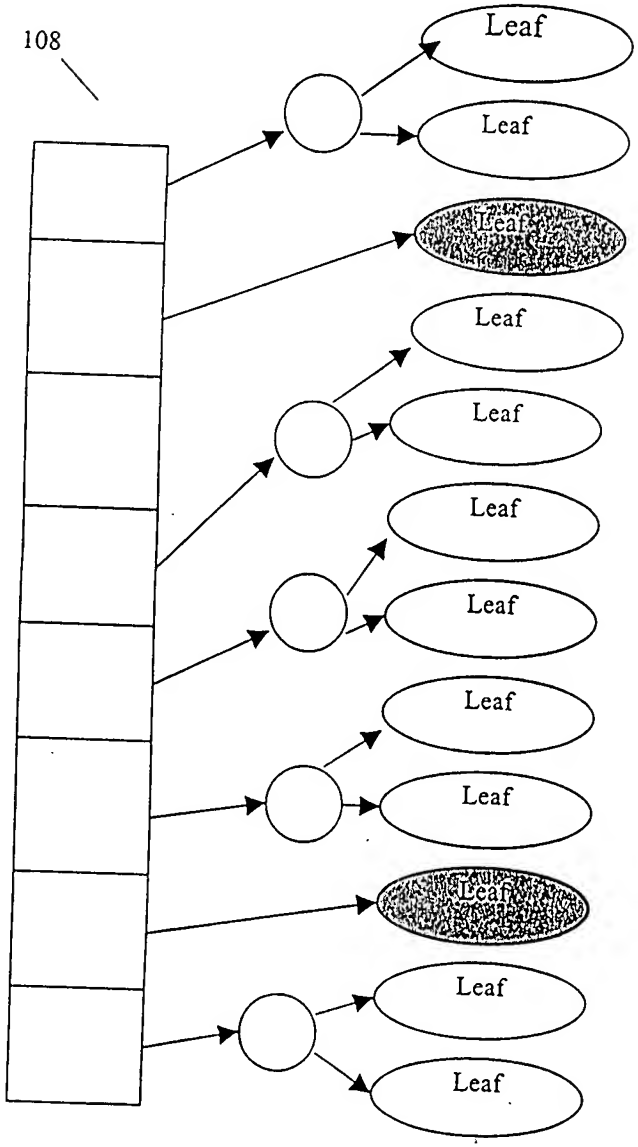


Datastructure without using a Direct Table



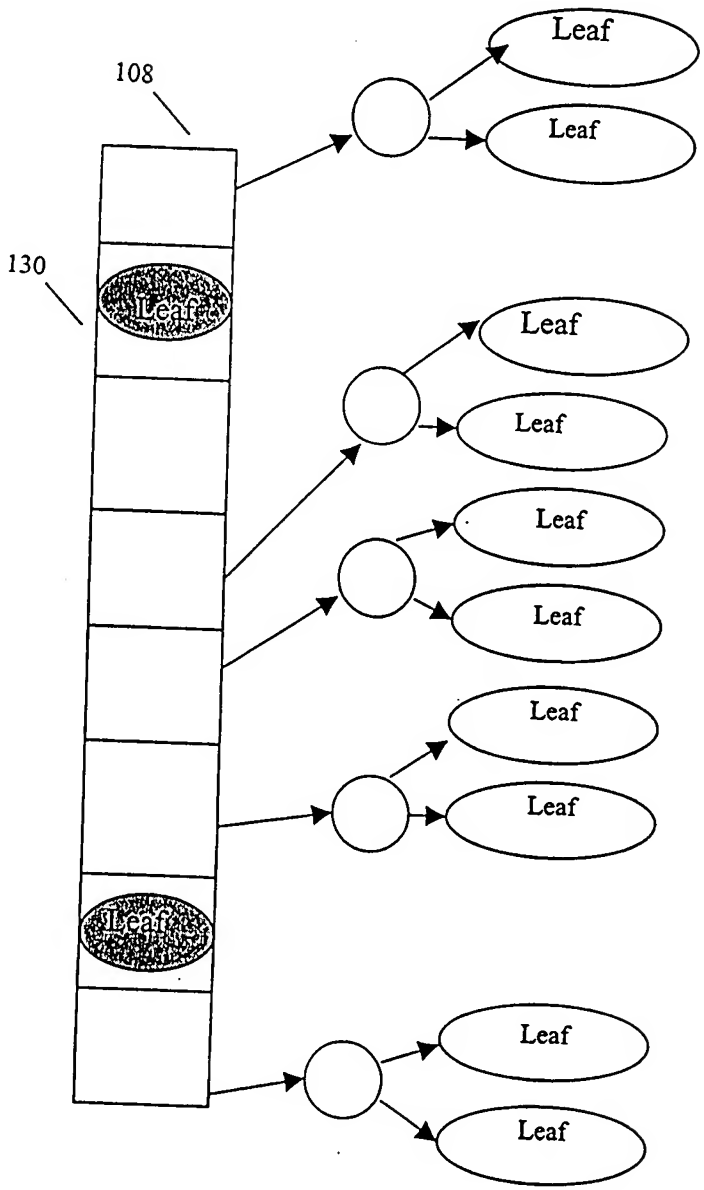
Datastructure with using a Direct Table

FIG. 6



Datastructure without Direct Leaves

FIG. 7



Datastructure with Direct Leaves

RA9-1999-0139-US1
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Format	Conditions	Valid in DTEntry ?	Valid in PSCB?	Format (2bits)	NPA/LCBA (26 bits)	NBT (8 bits)
Empty DTEntry	No leaves	Yes	No	00	0	0
Pointer to next PSCB	DtEntry contains pointer	Yes	Yes	00	NPA	NBT
Pointer to leaf	Single leaf associated with DTEntry; LCBA field contains pointer	Yes	Yes	01	LCBA	0

Fig. 8

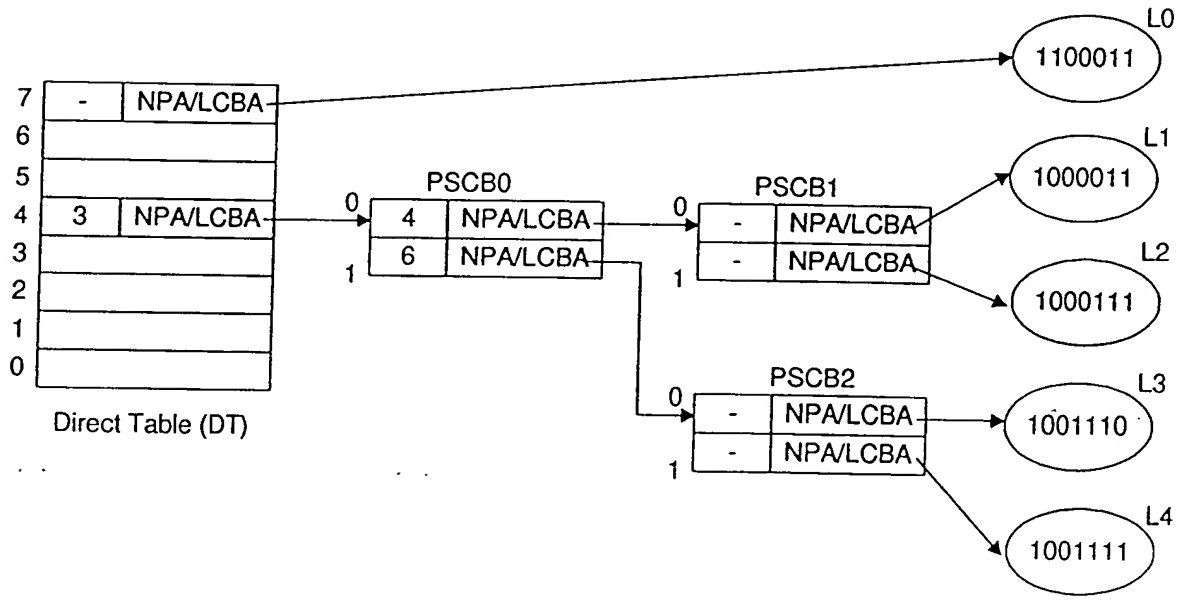

Fig. 9

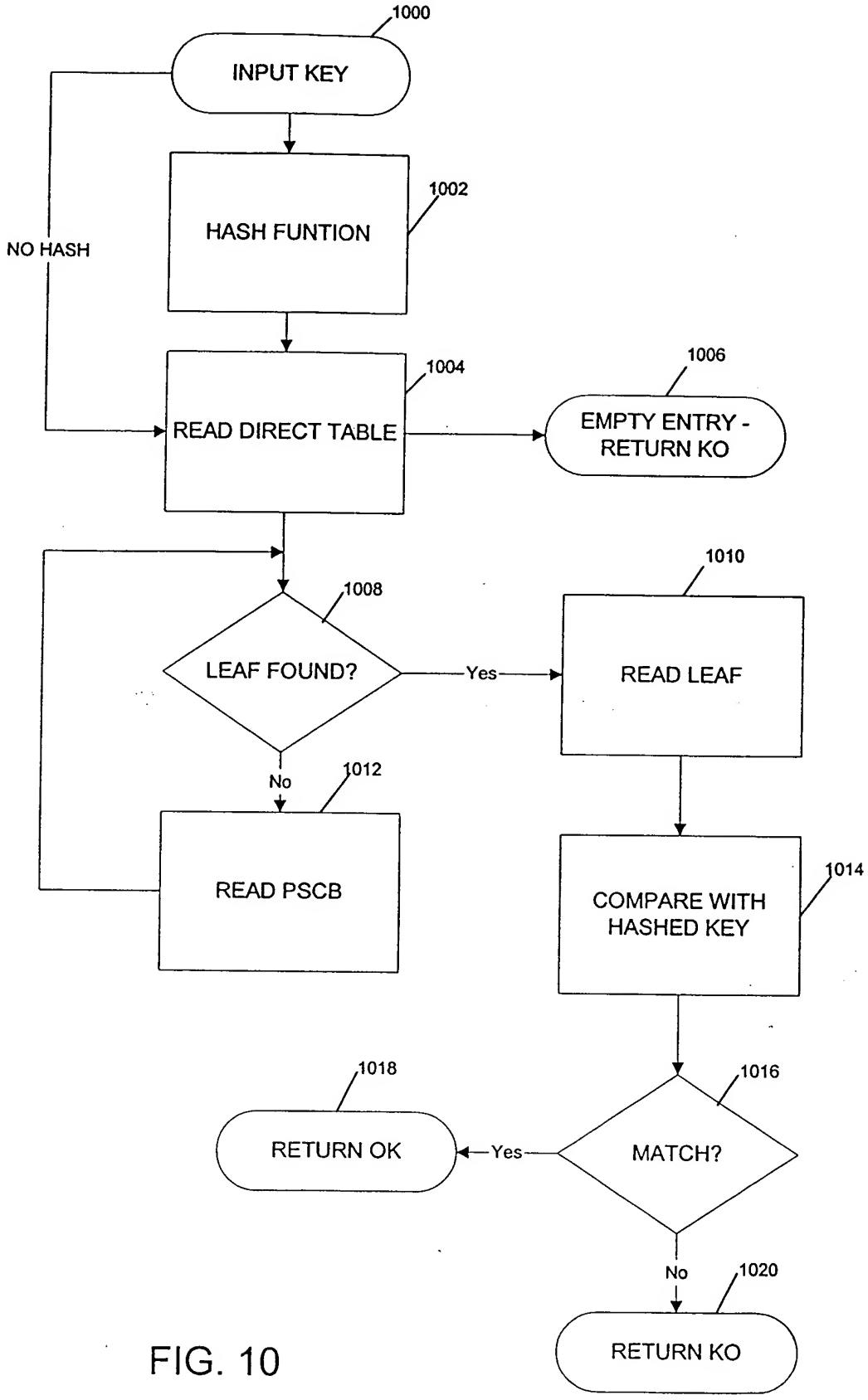
1000
INPUT KEY
HASH FUNTION
1002
NO HASH
1004
READ DIRECT TABLE
1006
EMPTY ENTRY - RETURN KO
1008
LEAF FOUND?
Yes
1010
READ LEAF
No
1012
READ PSCB
1014
COMPARE WITH HASHED KEY
1016
MATCH?
Yes
1018
RETURN OK
No
1020
RETURN KO

FIG. 10

LUDefTable Tree Definition

Field	Size	Bits
CacheEntry	1	0
Tree_Type	2	2..1
hash-type	4	6..3
color_en	1	7
PIP2_max_size	5	12 .. 8
NPARope_en	1	13
NPASMT_en	1	14
CompIndex_en	1	15
PSCB_fq_index	6	21 .. 16
PSCB_Height	1	22
Mask_Vector_En	1	23
CompIndex	8	31..24
DT_base_addr	26	57 .. 32
DT_size	4	61 .. 58
DT_interleaf	2	63 .. 62
Leaf_fq_index	6	69 .. 64
Leaf_Width	2	71 .. 70
Leaf_Height	3	74 .. 72
DirectLeafEn	1	75

FIG. 11

Field	Size	Address in TSM where PSCB is located
NPA0	26	Next PSCB address: pointer to next PSCB in the tree for 0-part of PSCB
NBT0	8	Next bit to test for 0-part of PSCB
LCBA0	26	Leaf control block address: pointer to leaf for 0-part of PSCB
NPA1	26	Next PSCB address: pointer to next PSCB in the tree for 1-part of PSCB
NBT1	8	Next bit to test for 1-part of PSCB
LCBA1	26	Leaf control block address: pointer to leaf for 1-part of PSCB
Index	8	Index of this PSCB (physically stored in the previous PSCB)
PatBit	1	The value of HashedKey[Index], based on the value of the Index field in the PSCB register

FIG. 12

Field Name	Length	Description
NLARope	4 bytes	Leaf chaining pointer, aging information and direct leaf information
Prefix_Len	1 byte	This field is not used by the TSE for FM trees and can be used by picocode
pattern	2 - 18 bytes	Pattern to be compared with the HashedKey
UserData	variable	The contents of this field is under complete picocode control; the UserData field can include one or more counters

FIG. 13

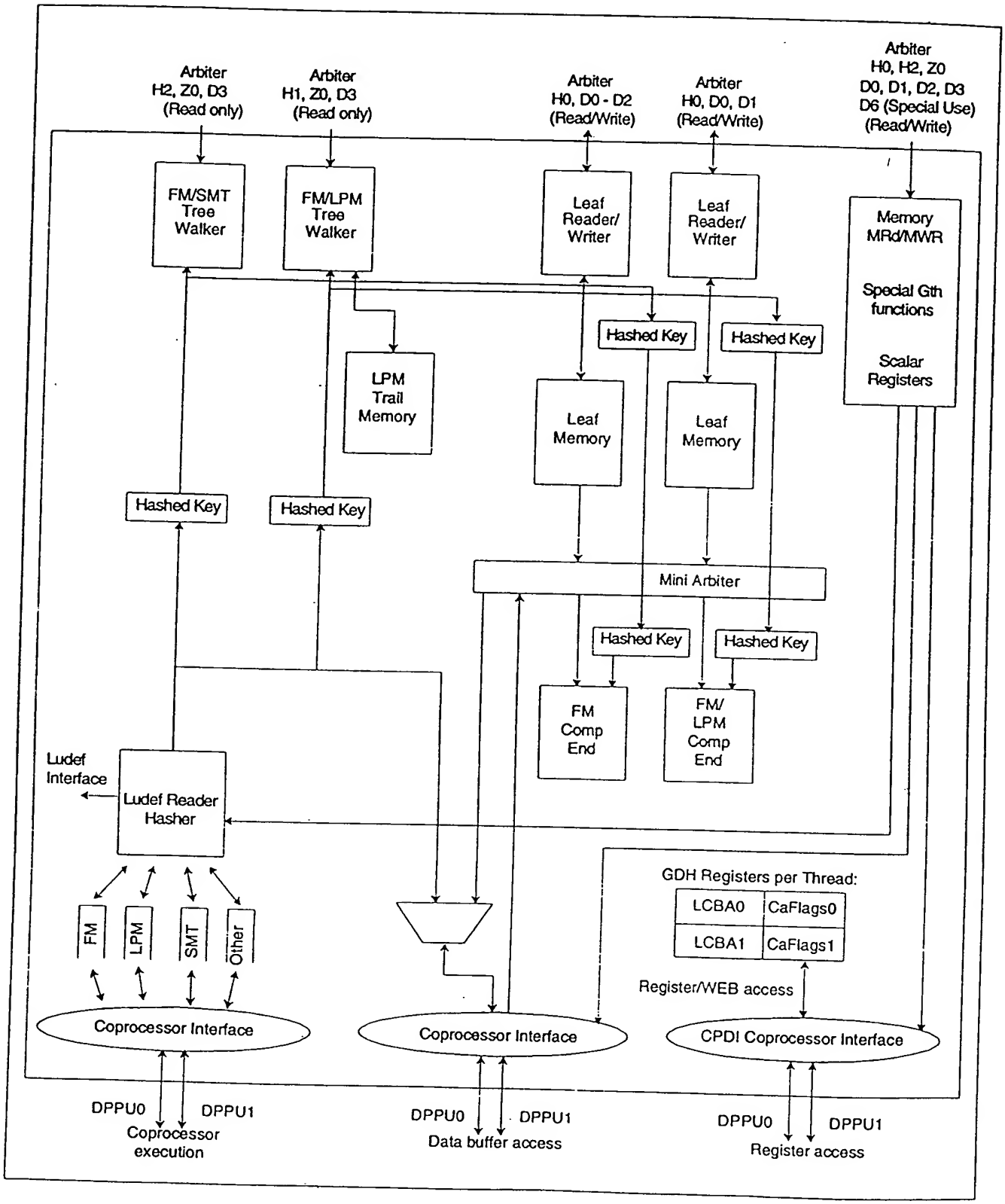
Arbiter
H2, Z0, D3
(Read only)
Arbiter
H1, Z0, D3
(Read only)
Arbiter
H0, D0 - D2
(Read/Write)
Arbiter
H0, D0, D1
(Read/Write)
Arbiter
H0, H2, Z0
D0, D1, D2, D3
D6 (Special Use)
(Read/Write)
FM/SMT Tree Walker
FM/LPM Tree Walker
Leaf Reader/ Writer
Leaf Reader/ Writer
Memory MRd/MWR
Special Gth functions
Scalar Registers
Hashed Key
Hashed Key
LPM Trail Memory
Leaf Memory
Leaf Memory
Hashed Key
Hashed Key
Mini Arbiter
Hashed Key
Hashed Key
FM Comp End
FM/ LPM Comp End
Ludef Interface
Ludef Reader Hasher
FM
LPM
SMT
Other
GDH Registers per Thread:
LCBA0
CaFlags0
LCBA1
CaFlags1
Register/WEB access
Coprocessor Interface
Coprocessor Interface
CPDI Coprocessor Interface
DPPU0
DPPU1
Coprocessor execution
DPPU0
DPPU1
Data buffer access
DPPU0
DPPU1
Register access

FIG. 14